REMARKS

Claims 1-22 are now pending in the application. Claims 1 and 9 are amended. The amendments to the claims are disclosed in the specification and Figures of the present application and thus do not introduce new matter. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

Applicant would like to thank the Examiner for courtesy extended during the interview on May 24, 2007. During the interview, the Examiner agreed that the above amendments distinguish over the prior art of record subject to further consideration and/or search.

REJECTION UNDER 35 U.S.C. § 112

Claim 9 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter which Applicant regards as the invention. The Examiner states that Claim 9 lacks antecedent basis for "internal frame buffer" and "external frame buffer". Claim 9 is amended to change "internal frame buffer" and "external frame buffer" to "internal memory array" and "external memory array", respectively. Thus, the 35 U.S.C. § 112 rejection should now be withdrawn.

REJECTION UNDER 35 U.S.C. § 103

Claims 1, 3-8, 16-18, and 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa (U.S. Pat. No. US006393520B2) in view of Takala

(U.S. Pat. No. US006909434B2), further in view of Pope (U.S. Pat. No. US005847705A).

With respect to Claim 1, Yoshikawa, Takala, and Pope fail to show, teach or suggest a control circuitry to copy display data from an external frame buffer to an internal frame buffer during reading of the same display data by a display controller from the external frame buffer.

The Examiner admits that Yoshikawa, Takala, and Pope fail to show, teach or suggest simultaneously copying display data into an internal memory array from an external memory array and reading the same display data by a display from the external memory array.

As best understood by Applicant, Yoshikawa discloses a data processing unit that includes a video controller. The video controller performs a data exchange between an internal memory and an external memory. See Abstract and col. 6, lines 20-64 of Yoshikawa. A data exchange is performed such that data that requires longer processing time or data that is more frequently accessed is mapped into the internal memory. During the data exchange, data in the internal memory is exchanged with data in the external memory. Thus, the data in the internal memory is not maintained in the external memory. The data in the internal memory is not the same as the data in the external memory. Also, the data transferred to the internal memory from the external memory is not also transferred from the external memory to a display. In Yoshikawa, data in the external memory, which is transferred to a display, is not also transferred to the internal memory.

The Examiner admits that Yoshikawa does not teach the limitation of after the display data is copied, the same display data is located in the internal frame buffer and the external frame buffer until a new frame is available in the external frame buffer. The Examiner alleges that Takala discloses this limitation.

As further best understood by Applicant, Takala discloses an integrated circuit with a local frame buffer and a display with a display frame buffer. Takala discloses a data transfer from the local frame buffer to the display frame buffer. In Col. 2, Lines 1-19, Takala states that display information is transferred from a processor to the local frame buffer, followed by updating the display frame buffer by transferring the display information from the local frame buffer to the display frame buffer. The stated section is silent with respect to maintenance of the same data in the local frame buffer and the display frame buffer. Nevertheless, Takala clearly does not state that data is transferred from the local frame buffer to the display. In Takala, data is transferred from the local frame buffer to the display frame buffer and then to the display.

As further best understood by Applicant, Pope discloses a pseudo screen buffer and a previous image buffer. When contents of the pseudo screen buffer are different than contents of the image buffer, contents at differing memory locations of the pseudo screen buffer are copied to the image buffer. This occurs at preselected timer interrupt intervals. Note that this is also different than the copying of data between external and internal memories while reading of the same data by a display controller from the external memory. Applicant is unable to find disclosure in Pope for the copying of data between the pseudo screen buffer and the image buffer while reading the same data by a display controller from one of the buffers.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. The relied upon references alone or in combination fail to teach or suggest each and every element claimed.

Therefore, Claim 1 is allowable for at least these reasons. Claim 16 is allowable for at least similar reasons as Claim 1. Claims 3-8, 17-18, and 20-22 ultimately depend from Claims 1 and 16 and are allowable for at least similar reasons.

Claims 9, 11, and 13-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa (U.S. Pat. No. US006393520B2) in view of Takala (U.S. Pat. No. US006909434B2), further in view of Cross (U.S. Pat. No. US006108015A), further in view of Pope (U.S. Pat. No. US005847705A).

With respect to Claim 9, Yoshikawa, Takala, Cross and Pope fail to show, teach or suggest the limitations of a data copy circuitry that enables data from an external memory array to be copied to an internal memory array during a new frame display refresh operation. The new frame display refresh operation includes reading the data by a display controller from the external memory array.

Claim 9 distinguishes over Yoshikawa, Takala, and Pope for at least similar reasons as Claim 1.

Furthermore, as best understood by Applicant, Cross discloses an internal frame buffer, an external frame buffer, a display controller, and a display. Data from the internal frame buffer and from the external frame buffer is provided to the display controller in performing a screen refresh. Applicant is unable to find disclosure in Cross

for the copying of data from the external frame buffer to the internal frame buffer or for the performance of such copying while reading the external frame buffer by the display controller.

Therefore, Claim 9 is allowable for at least the above reasons. Claims 11 and 13-15 ultimately depend from Claim 9 and are allowable for at least similar reasons.

ALLOWABLE CLAIMS

Claims 2, 10, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant reserves the right to rewrite these claims into their originally allowable form at a later date if needed.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: June 27, 2007

By: _____
Michael D. Wiggins
Reg. No. 34,754

Jeffrey J. Chapp
Reg. No. 50,579

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

MDW/JJC/mrg